

U.S. Patent Application No. 10/538,905
Response to Office Action dated August 27, 2007

1 – 15. (Canceled)

16. (Currently Amended) A method according to claim 15 for fabricating a three-dimensional integrated device including a plurality of vertically stacked and interconnected wafers, the method comprising the steps of:

providing a first wafer having a front surface and a back surface, the first wafer having devices formed in a region adjacent to the front surface thereof;

forming a via in the first wafer extending from the front surface, the via being characterized by a lateral dimension at the front surface;

removing material from the first wafer at the back surface thereof;

forming an opening in the back surface of the first wafer, thereby exposing the via, the opening having a lateral dimension greater than said lateral dimension of the via;

forming a layer of conducting material in said opening;

providing a second wafer having a front surface and a back surface, the second wafer having devices formed therein adjacent to the front surface thereof;

forming a stud on the front surface of the second wafer;

forming a layer of bonding material on the front surface of the second wafer, the studs projecting vertically therefrom;

aligning the stud to the opening in the back surface of the first wafer; and

bonding the second wafer to the first wafer using the layer of bonding material, so that the stud makes electrical contact with the via, further comprising the steps of:

forming a via in the second wafer extending from the front surface thereof, the via being characterized by a lateral dimension at the front surface;

removing material from the second wafer at the back surface thereof;

forming an opening in the back surface of the second wafer, thereby exposing the via therein, said opening having a lateral dimension greater than said lateral dimension of the via;

forming a layer of conducting material in said opening;

providing a third wafer having a front surface, the third wafer having devices formed therein adjacent to the front surface thereof;

forming a stud on the front surface of the third wafer;

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forming a layer of bonding material on the front surface of the third wafer, the studs projecting vertically therefrom;

aligning the stud to the opening in the back surface of the second wafer; and
bonding the third wafer to the second wafer using the layer of bonding material,
so that the stud of the third wafer makes electrical contact with the via of the second
wafer, with the stud of the second wafer, and with the via of the first wafer.

17. (Currently Amended) A method according to ~~claim 15 or claim 16~~,
wherein said step of removing material causes the wafer to have a thickness of less than
20 μ m.

18. (Currently Amended) A method according to ~~claim 15 or claim 16~~, further
comprising the step of attaching a handling plate to the front surface of the first wafer
using a layer of bonding material.

19. (Currently Amended) A method according to ~~claim 15 or claim 16~~, further
comprising the step of forming a conducting body in one of the first wafer and the second
wafer and connecting to the via in the first wafer, the conducting body extending laterally
under the devices of the first wafer, and wherein the opening in the back side of the first
wafer is separated laterally from the via in accordance with the lateral extent of the
conducting body.

20. (Currently Amended) A method according to ~~claim 15 or claim 16~~, further
comprising the steps of:

forming an additional opening in the back surface of the first wafer;
forming an additional layer of conducting material in said additional opening;
forming an additional stud on the front surface of the second wafer; and
aligning the additional stud to the additional opening in the back surface of the
first wafer; and wherein said step of bonding the second wafer to the first wafer forms a
connection between the additional stud and the additional layer of conducting material for
conducting heat between the second wafer and the first wafer.

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21. (Original) A method according to claim 20, wherein the additional layer of conducting material is electrically insulated from the via.

22. (Original) A method according to claim 16, further comprising the steps of:

forming an additional opening in the back surface of the second wafer;
forming an additional layer of conducting material in said additional opening;
forming an additional stud on the front surface of the third wafer; and
aligning the additional stud to the additional opening in the back surface of the second wafer;

and wherein said step of bonding the third wafer to the second wafer forms a connection between the additional stud and the additional layer of conducting material for conducting heat between the third wafer and the second wafer.

23. (Currently Amended) A method according to ~~claim 15 or claim 16~~, wherein said bonding material is a thermoplastic material.

24. (Original) A method according to claim 23, wherein the thermoplastic material is polyimide.

25. (Currently Amended) A method according to ~~claim 15 or claim 16~~, further comprising the step of attaching the three-dimensional integrated device to a multichip module.

26. (Currently Amended) A method according to ~~claim 15 or claim 16~~, further comprising the step of attaching the three-dimensional integrated device to an insulating layer having wiring formed therein using a stud-via connection.

27. (Original) A method according to claim 16, wherein the first wafer and second wafer have cache memory devices, and the third wafer has logic devices.

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28. (Original) A method according to claim 16, wherein at least one of the first wafer, the second wafer and the third wafer includes a MEMS device.